

31011 U.S. PTO
10/08/789
02/25/02
2821/1882

PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10084789	FILING DATE 02 25 2002	CLASS 327	SUBCLASS	GAU 2816	EXAMINER
**APPLICANTS: Endo Masaki					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED: JAPAN P2001 050433 02 26 2001					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO			
35 USC 113 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		450100-03853			
Verified and Acknowledged Examiners initials					
TITLE : Delay lock loop circuit, variable delay circuit, and recording signal compensating circuit					

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	
		Print Claim for O.G.	
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
<input type="checkbox"/> TERMINAL DISCLAIMER		Application Examiner	
		PREPARED FOR ISSUE	
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